Prefabricated OFET Test Chips (Low Density)

User Manual

Manual version 2.0.A

Product code(s): S181, S183

Contents

Contents **2**
1. Specifications **3**
1.1 Silicon Substrates 3
1.2 Device Channel Design 3
2. Fabrication and Usage **4**
2.1 Handling 4
2.2 Cleaning 5
2.3 OFET fabrication 6
2.3.1 Surface pre-treatments 6
2.3.2 Removal of excess semiconductor 7
3. List of Associated Products **9**
4. Contact Details **10**
5. Revision History **10**

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1. Specifications

1.1 Silicon Substrates

The OFET test chips are fabricated using the following products from Ossila:

- Silicon Oxide Substrates (S146)
- Source-Drain Deposition Masks for Low-Density OFETs
- Evaporation Stack for Low-Density OFETs (E281)

The silicon oxide substrates (SiO_2) are cut from a highly P-doped (boron) silicon wafer coated with a 300 nm thick layer of SiO_2 on both sides. Specifically designed for OFET testing and material screening, the doped silicon and the oxide layer provide the gate and the dielectric respectively for a bottom-gate, bottom-contact architecture

Size	20 mm × 15 mm
Substrate Thickness	725 ± 25 µm
Growth	CZ
Orientation	<100>
Type/Dopant	P/Boron
Resistivity	5×10^{-4} to 10^{-2} Ω/cm
Front Surface	Polished
Back surface	Unpolished
Oxide Thickness (SiO_2)	300 nm
Capacitance	1.09×10^{-8} F/ cm^2

1.2 Device Channel Design

Substrate	Doped Silicon/Silicon Oxide	
Device architecture	Bottom Gate, Bottom Contact	
S-D adhesion layer	Cr (2 nm)	
S-D electrode material	Au (70 nm)	
Product Code	S181	S183
Channel Type	Linear, constant	Linear, variable
Channel Length	30 µm	30, 40, 50, 60, 80 µm

There are five devices per substrate.

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The structure and key features of the linear, low-density, constant-length channel, prepatterned OFET substrate are detailed in the schematic in Figure 1.1. The channel bar tolerance is ±8 µm.

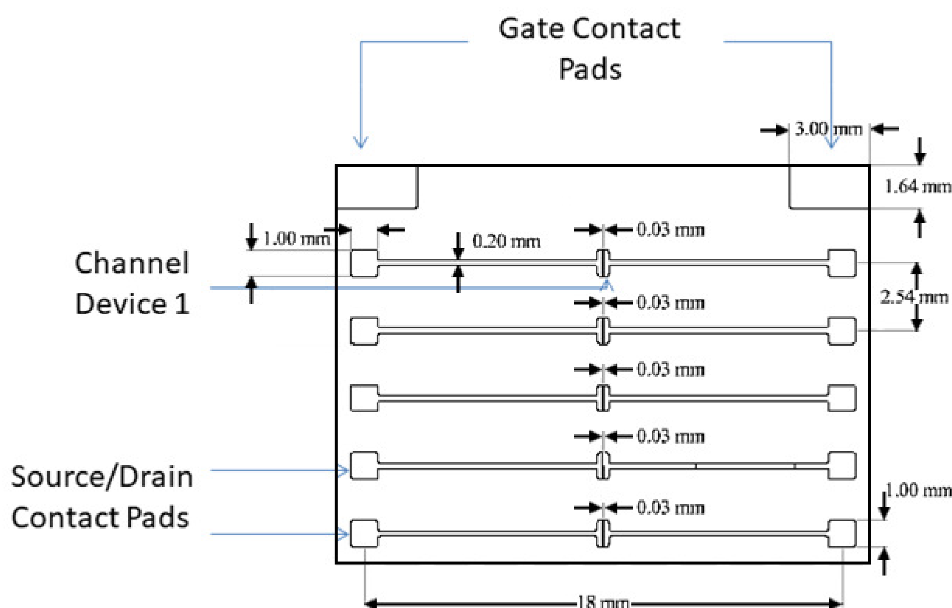

Figure 1.1. Schematic of linear, low-density, constant-channel-length, pre-patterned silicon substrate (S181).

2. Fabrication and Usage

2.1 Handling

Figure 1.1 shows a schematic of the different areas of the LD OFET test chips.

(I) Substrate areas:

1. Gate
2. Contact pad
3. Central area
4. Active area/OFET channels
5. Lateral edge

The substrate must be handled with care on the gate, preferably using rounded, flat tipped tweezers such as Type 2A (C121). Use of pointed tip tweezers increases the risk of inadvertently damaging the patterned metallic features or cracking the silicon substrate and silicon oxide dielectric which is very brittle.

Areas 1 and 2 are relatively robust and can be handled by tweezers and wiped clean with cotton buds. However, any mechanical contacts within the active area (area 3 to 5) may damage the channel and

hence affect the device performance. Excessive tweezer pressure may also damage the drain/source pads and, especially the narrow “bridges” connecting the pads with the transistor channel.

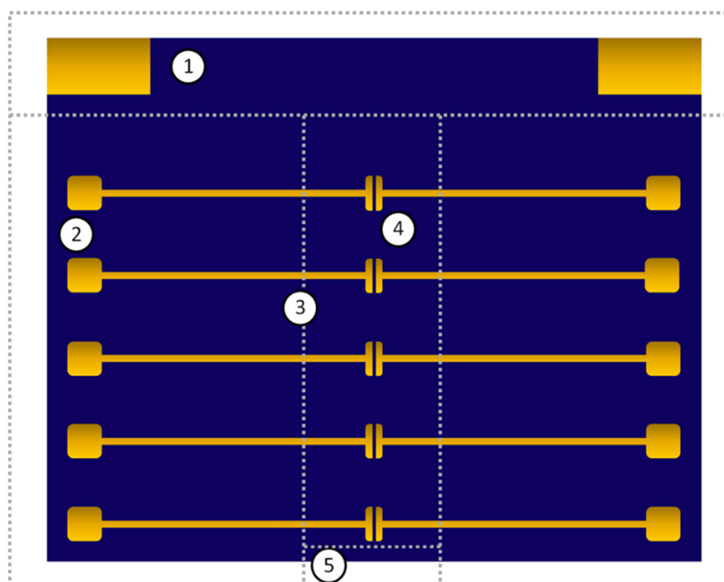

Figure 2.1. Low-density, pre-patterned OFET test chip schematic. 1: Gate electrode top edge and contact pads; 2: source-drain contact pads; 3: Central area; 4: active area/OFET device channels; 5: lateral edge.

2.2 Cleaning

Before starting the fabrication routine, make sure that the surface is clean and free of dust.

(I) First use

The substrates are nominally clean out of their packaging, however it is advisable to rinse them in a volatile organic solvent such as Isopropyl alcohol, acetone or butanone and blow dry with compressed nitrogen.

(II) Reuse

The test chips have been designed to be able to be reused for (at least) three or four fabrication cycles. If carefully handled, and depending on the fabrication/surface treatment used, the substrates can be re-used provided all of the previous material has been removed. It is advisable to only re-use substrates for internal parameter testing and to use brand new substrates when data suitable for publication is required.

1. Rinse the substrates with a solvent that can dissolve the material that has been deposited.
2. Use an oxidising method such as UV ozone treatment or oxygen plasma treatment to remove all trace organic material.

(III) Conditions to avoid

- Do not use a detergent, such as Hellmanex III, because this may etch the patterned features.

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- Do not wipe the device channel (4) with cleanroom swabs because this may damaged the channel.
- Do not soak or sonicate the test chips for extended periods of time in organic solvents, particularly chlorinated solvents, because this can weaken the adhesion of the gold channels and contact pads. Ensure that all solvent has evaporated before subjecting the test chips to mechanical stress.

2.3 OFET fabrication

The Prefabricated OFET Test Chips are suitable for OFET fabrication by wet processing techniques such as spin coating, dip-coating or drop casting or vapour processing such as thermal evaporation of organic semiconductors.

2.3.1 Surface pre-treatments

The surface of silicon oxide is full of electron charge traps that hinder charge transport for p-type semiconductors and make it impossible to characterise n-type semiconductors. OTS, or octadecyltrichlorosilane, is a molecule that readily forms strong covalent bonds with polar substrate surfaces such as silicon oxide to form self-assembled monolayers. The layer of self-assembled OTS passivates the surface of the silicon oxide, reducing the impact of the charge traps.

Ossila use a 1 mM solution of OTS in cyclohexane to soak the pre-activated substrates in for 20 minutes. This recipe gives a water contact angle of up to 90 degrees. Other methods of OTS treatment are available using different concentrations, solvents etc. as seen in the literature. These methods can result in a larger water contact angle, better surface passivation and increased charge transport. However a larger water contact angle also makes the substrate much more difficult to wet and therefore much more difficult to deposit the semiconductor onto.

OTS itself is very moisture sensitive, so should be stored and handled under inert gas if possible (such as a nitrogen-filled glovebox). Pure OTS will react with moisture in the air and polymerise resulting in a white powder residue within seconds. If there is not a glovebox available, The OTS can be stored in a refrigerator sealed with parafilm. The reaction with moisture in the air is slower when the OTS is cold, so some OTS can be quickly pipetted straight into a small vial of cyclohexane/solvent without too much degradation of the OTS in the bottle.

(I) Surface activation

To achieve a uniform self-assembled monolayer (SAM), a uniform substrate surface energy is needed. For silicon dioxide surfaces, this means fully oxidising the surface into hydroxyl terminating groups so that the surface is reactive to the OTS treatment.

Therefore we strongly recommend using a 5 minute UV ozone treatment after solvent cleaning, or 30 seconds with oxygen plasma.

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(II) OTS treatment

The procedure is carried out in a fume cupboard under normal atmospheric conditions. The chemical reaction that generates the SAM of OTS on the substrate surface requires a very small quantity of water. Moisture present in the air is enough for this.

The Ossila Annealing and Cleaning Beaker (C191) and Substrate Rack for Cleaning and Storage (E101) are used to treat the substrates, which allows a large number of substrates to be treated at once, safely. Additionally, the annealing beaker has a glass slide lid that prevents further ingress of air/moisture that may interfere with the reaction.

A small, dry glass vial of OTS solution is prepared in the glovebox (approximately 25 microlitres of OTS inside 1 ml of anhydrous cyclohexane). This effectively dilutes the OTS so that it does not immediately react in air when adding it to the annealing beaker.

The substrates are loaded into the substrate rack and placed into the annealing beaker. When the beaker contains the substrate rack and substrates, the volume of remaining space is approximately 60 ml. The beaker is filled close to the top with cyclohexane. The small vial of OTS solution is added to the solvent in the beaker and the glass lid slid to cover most of the beaker. The remaining air space is carefully filled with cyclohexane such that when the beaker is completely covered there is no air bubbles remaining.

The beaker is left for 20 minutes. The substrate rack is removed using tweezers and put through 2x dump rinses in fresh cyclohexane. The washed substrates are blown dry using a nitrogen gun before annealing on a hotplate at 150 °C for 5 minutes and leaving to cool to room temperature slowly.

The substrates are now ready to treat with semiconductor.

2.3.2 Removal of excess semiconductor

If the semiconductor is applied wet coating techniques, the gate and drain/source areas must be wiped clean using Standard Cleanroom Swabs wetted with the appropriated solvent.

(I) Standard cleaning

Make sure that the *central area* (3 – the active area and the gold electrical bridges from Figure 2.1) is not wiped.

Note: The chromium adhesion layer should guarantee sufficient adherence to allow for gentle cleaning of the gold bridge in the central area.

The lateral edge of the test chip (see area 5 from Figure 2.1) must be carefully cleaned because it can be the source of non-negligible gate leakage. In order to clean this area effectively without damaging the devices, the following routine should be followed:

- Place the substrate on an absorbent surface such as cleanroom tissue and hold it firmly with tweezers

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- Position a cleanroom swab tip (wet with the appropriate solvent) perpendicular to the surface, next to the lateral edge.
- Incline the cotton bud at an angle of 70-80° toward the substrate surface and move it along the edge a few times.

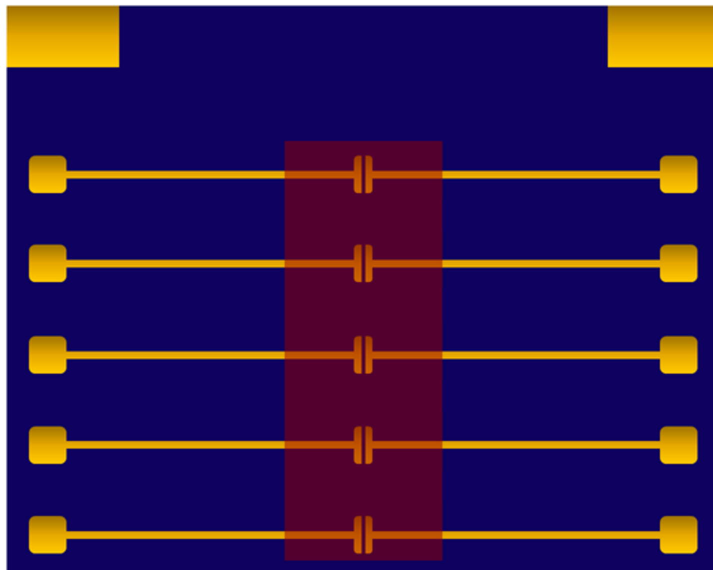

Figure 2.2. Visualisation of OFET test chip after Standard cleaning.

(II) High-precision cleaning

To avoid cross-talk between devices, it is advised to remove the semiconductor between devices. This can be achieved by careful use of the pointed (high-precision) cleanroom swabs. Figure 2.3 shows what the completed test chip should look like after wiping.

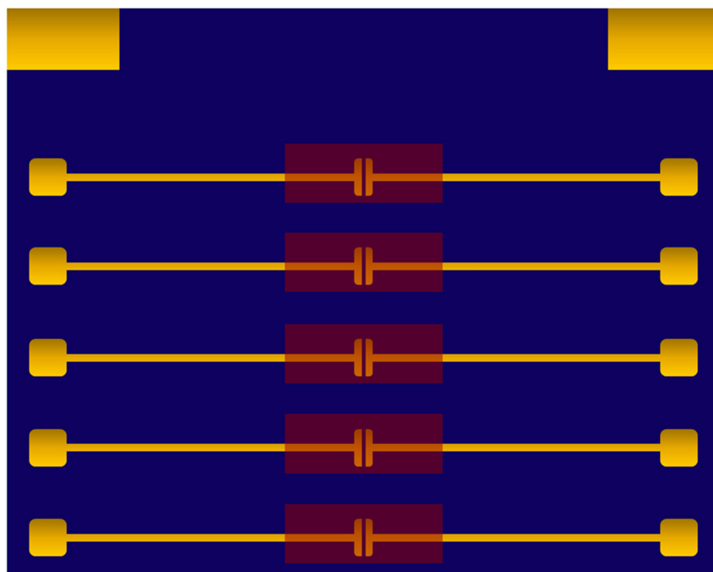

Figure 2.3. Visualisation of OFET test chip after high-precision cleaning.

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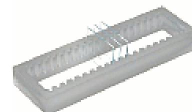
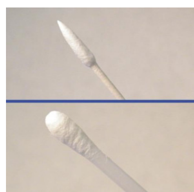
3. List of Associated Products

Related accessories

Annealing and Cleaning Beaker (C191)
Polypropylene beaker with glass lid ideal for experiments where enclosed volumes and minimal solvent use are required.



Substrate Rack for Cleaning and Storage (E101)
Holds 20 substrates. Injection moulded from polypropylene to be chemically resistant to all common solvents and acids.



Cleanroom Swabs (C202 and C202)
High-precision and standard swabs with minimal particle shedding.

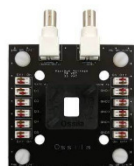
Precision Tweezers (C121 and C122)
Having the right tweezers is essential for handling substrates effectively, safely, and securely.

Related processing equipment

UV Ozone Cleaner (L2002A2)
For removing contamination on the surface of samples, providing you with ultraclean surfaces within minutes to spin coat onto.

Contact Angle Goniometer (L2004A1)
Fast, reliable, and easy measurement of the contact angle of a droplet on a surface. The system has a low price, compact size and intuitive PC software included.

Related test equipment



OFET Test Board for Low Density OFETs (E222)
High-precision measurements of up to five OFETs on a single substrate to help measure more experimental parameters more quickly.

Probe Station (E451)
Multi-purpose tool with 3 interchangeable probe heads, pre-aligned to speed up measurement.

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4. Contact Details

To the best of our knowledge the technical information provided here is accurate. However, Ossila assume no liability for the accuracy of this information. The values provided here are typical at the time of manufacture and may vary over time and from batch to batch.

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5. Revision History

Rev	Date	Description
A	May 2018	First publication

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