PLATINUM OFET TEST CHIPS

USER MANUAL

Manual version: 1.0.0
Product code: S403A1

Contents

1. Specifications

Table 1.1. Ossila Platinum OFET Test Chip specifications.

Geometry	Linear
Arrangement (S403A1)	20 electrode pairs, 5 channel widths
Arrangement (S403A2)	16 electrode pairs minimum, 4 channel widths minimum*
Channel width	1 mm
Channel lengths	2 (S403A1 only), 4, 6, 8, and 10 µm
Device architecture	Bottom gate, bottom contact
Substrate / Gate	Silicon (p-doped)
Gate dielectric	300 nm thermally grown silicon dioxide
Source-Drain electrodes	Platinum (100 nm) / Titanium adhesion layer (5 nm)
Deposition method	Plasma sputtering
Patterning method	Photolithography

*Please note that the fabrication and layout of S403A1 and S403A2 is identical, however one or more of the 2 µm channels may not be fully resolved on the S403A2 substrates (as highlighted with the red dotted border in the figure below). All four 2 µm channels are present on the S403A1 substrates. The S403A2 substrates may have some cosmetic defects (edge chips, minor surface scratches) that will not affect device performance.

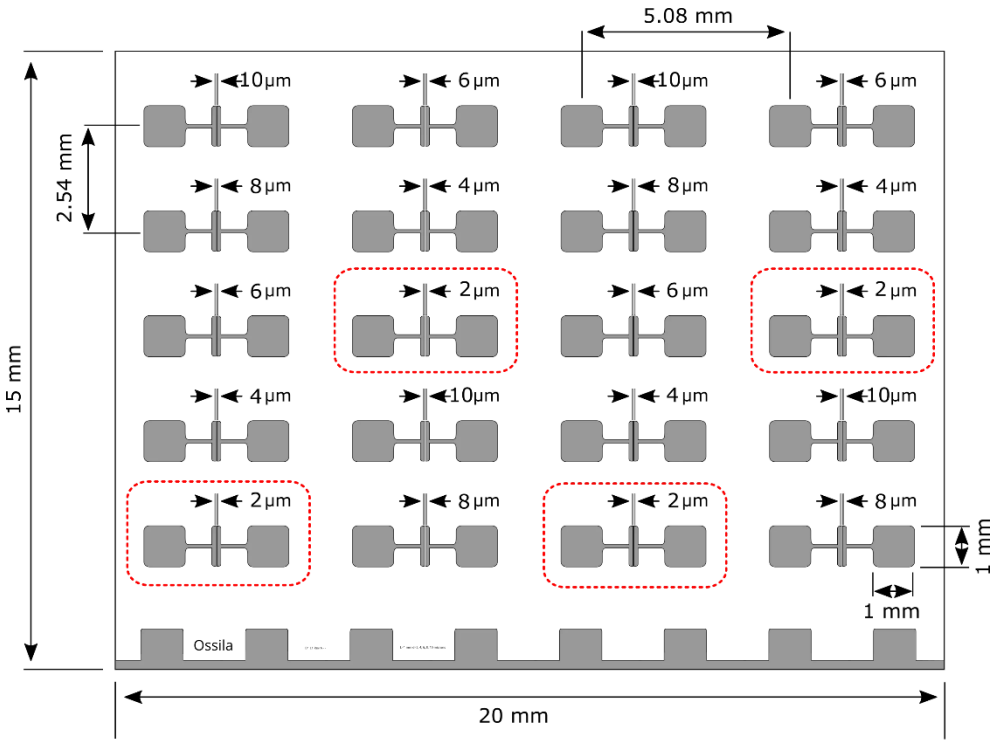

Figure 1.1. Schematic diagram of the platinum OFET test chip. Highlighted channels in red boxes are not guaranteed to be functional on S403A2.

2. Handling

(I) Substrate areas:

1. Gate electrode
2. Source-drain contact pad
3. Central area
4. Active area/OFET channel
5. Lateral edge

The substrate must be handled with care on the gate, preferably using rounded, flat tipped tweezers such as Type 2A (C121). Use of pointed tip tweezers increases the risk of inadvertently damaging the patterned metallic features or cracking the silicon substrate and silicon oxide dielectric which is very brittle.

Areas 1 and 2 are relatively robust and can be handled by tweezers and wiped clean with cotton buds. However, any mechanical contacts within the active area (area 3 to 5) may damage the channel and hence affect the device performance. Excessive tweezer pressure may also damage the drain/source pads and, especially the narrow “bridges” connecting the pads with the transistor channel.

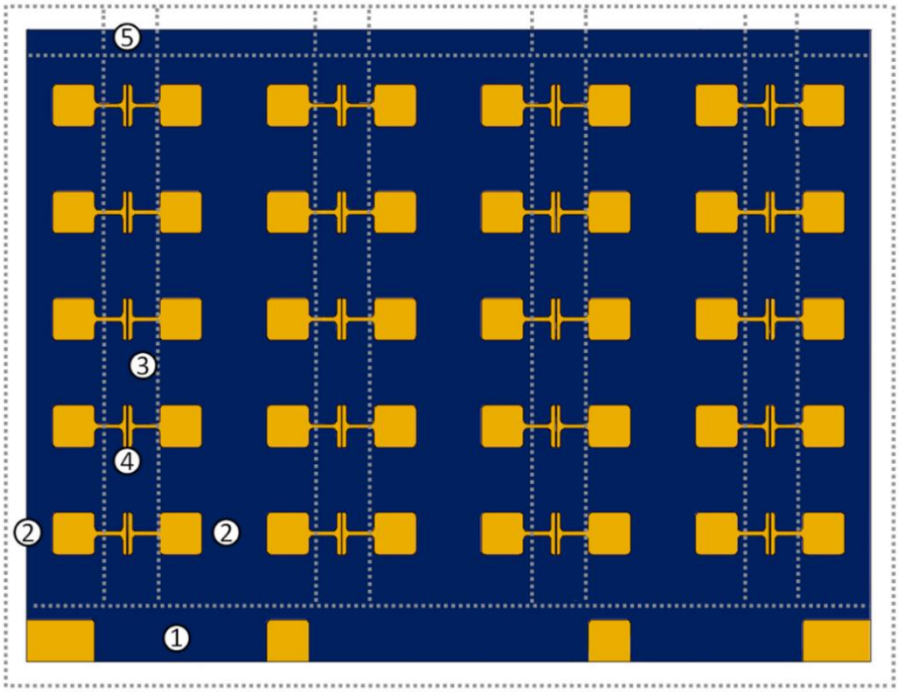

Figure 2.1. OFET test chip areas: 1) gate electrode top edge and contact pads; 2) source-drain contact pads; 3) central area; 4) active area/OFET device channels; 5) lateral edge.

3. Cleaning

Before starting the fabrication routine, make sure that the surface is clean and free of dust.

3.1 First Use

The substrates are nominally clean out of their packaging; however, it is advisable to rinse them in a volatile organic solvent such as Isopropyl alcohol, acetone or butanone and blow dry with compressed nitrogen.

3.2 Re-Use

The test chips have been designed to be able to be reused for (at least) three or four fabrication cycles. If carefully handled, and depending on the fabrication/surface treatment used, the substrates can be re-used provided all the previous material has been removed. It is advisable to only re-use substrates for internal parameter testing and to use brand new substrates when data suitable for publication is required.

1. Rinse the substrates with a solvent that can dissolve the material that has been deposited.
2. Use an oxidising method such as UV ozone treatment or oxygen plasma treatment to remove all trace organic material.

3.3 Conditions to Avoid

- Do not use a detergent, such as Hellmanex III, because this may etch the patterned features.
- Do not wipe the device channel (4) with cleanroom swabs because this may damage the channel.
- Do not soak or sonicate the test chips for extended periods of time in organic solvents, particularly chlorinated solvents, because this can weaken the adhesion of the platinum channels and contact pads. Ensure that all solvent has evaporated before subjecting the test chips to mechanical stress.

4. OFET Fabrication

The Platinum OFET Test Chips are suitable for OFET fabrication by wet processing techniques such as spin coating, dip-coating or drop casting or vapour processing such as thermal evaporation of organic semiconductors.

4.1 Surface Pre-Treatment

The surface of silicon oxide is full of electron charge traps that hinder charge transport for p-type semiconductors and make it impossible to characterise n-type semiconductors. OTS, or octadecyltrichlorosilane, is an organometallic molecule that readily forms strong covalent bonds with polar substrate surfaces such as silicon oxide to form self-assembled monolayers. The layer of self-assembled OTS passivates the surface of the silicon oxide, reducing the impact of the charge traps.

Ossila recommends a 1 mM solution of OTS in cyclohexane to soak the pre-activated substrates in for 20 minutes. This recipe gives a water contact angle of up to 90 degrees. Other methods of OTS treatment are available using different concentrations, solvents etc. as seen in the literature. These methods can result in a larger water contact angle, better surface passivation and increased charge transport. However, a larger water contact angle also makes the substrate much more difficult to wet and therefore much more difficult to deposit the semiconductor onto.

OTS itself is very moisture sensitive, so should be stored and handled under inert gas if possible (such as a nitrogen-filled glovebox). Pure OTS will react with moisture in the air and polymerise resulting in a white powder residue within seconds. If there is not a glovebox available, The OTS can be stored in a refrigerator sealed with parafilm. The reaction with moisture in the air is slower when the OTS is cold, so some OTS can be quickly pipetted straight into a small vial of cyclohexane/solvent without too much degradation of the OTS in the bottle.

4.1.1 Surface Activation

To achieve a uniform self-assembled monolayer (SAM), a uniform substrate surface energy is needed. For silicon dioxide surfaces, this means fully oxidising the surface into hydroxyl terminating groups so that the surface is reactive to the OTS treatment.

Therefore, we strongly recommend using a 5-minute **UV ozone** treatment after solvent cleaning, or 30 seconds with oxygen plasma.

4.1.2 OTS Treatment

The procedure is carried out in a fume hood under normal atmospheric conditions. The chemical reaction that generates the SAM of OTS on the substrate surface requires a very small quantity of water. Moisture present in the air is enough for this.

The Ossila **Annealing and Cleaning Beaker** and **Substrate Rack** are used to treat the substrates, which allows many substrates to be treated at once, safely. Additionally, the annealing beaker has a glass slide lid that prevents further ingress of air/moisture that may interfere with the reaction.

A small, dry glass vial of OTS solution is prepared in the glovebox (approximately 25 microlitres of OTS inside 1 ml of anhydrous cyclohexane). This effectively dilutes the OTS so that it does not immediately react in air when adding it to the annealing beaker.

The substrates are loaded into the substrate rack and placed into the annealing beaker. When the beaker contains the substrate rack and substrates, the volume of remaining space is approximately 60 ml. The beaker is filled close to the top with cyclohexane. The small vial of OTS solution is added to the solvent in the beaker and the glass lid slid to cover most of the beaker. The remaining air space is carefully filled with cyclohexane such that when the beaker is completely covered there is no air bubbles remaining.

The beaker is left for 20 minutes. The substrate rack is removed using tweezers and put through 2 dump rinses in fresh cyclohexane. The washed substrates are blown dry using a nitrogen gun before annealing on a hotplate at 150 °C for 5 minutes and leaving to cool to room temperature slowly.

The substrates are now ready to treat with semiconductor.

4.2 Removal of Excess Semiconductor

If the semiconductor is applied wet coating techniques, the gate and drain/source areas must be wiped clean using cleanroom swabs wetted with the appropriated solvent.

4.2.1 Standard Cleaning

Make sure that the central area (3 – the active area and the platinum electrical bridges from (**Figure 2.1**) is not wiped.

> **Note:** The titanium adhesion layer should guarantee sufficient adherence to all for gentle cleaning of the platinum bridge in the central area.

The lateral edge of the test chip (see area 5 from **Figure 2.1**) must be carefully cleaned because it can be the source of non-negligible gate leakage. To clean this area effectively without damaging the devices, the following routine should be followed:

- Place the substrate on an absorbent surface such as cleanroom tissue and hold it firmly with tweezers
- Position a cleanroom swab tip (wet with the appropriate solvent) perpendicular to the surface, next to the lateral edge.
- Incline the cotton bud at an angle of 70-80° toward the substrate surface and move it along the edge a few times.

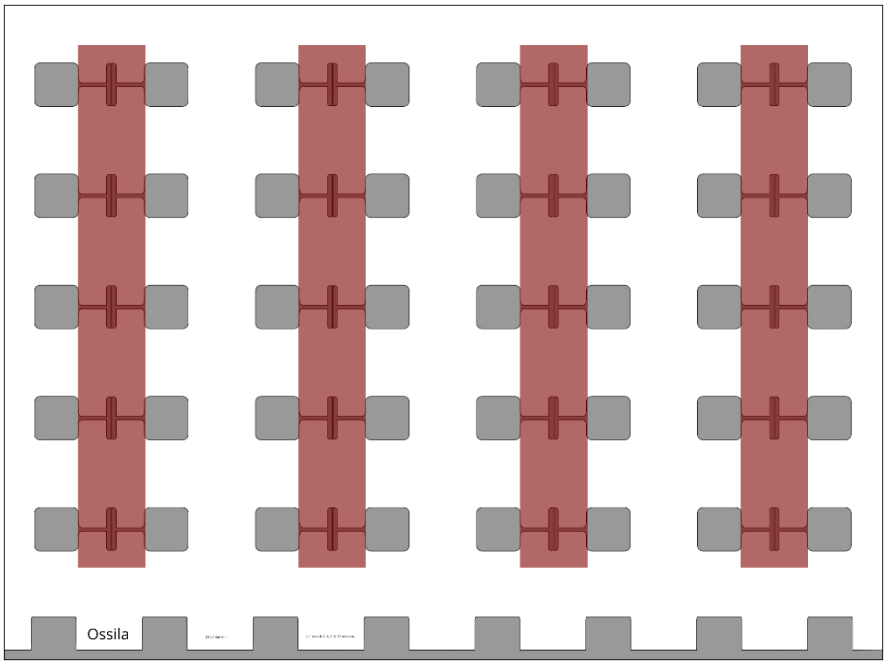

Figure 4.1. Visualisation of OFET test chip after standard cleaning.

4.2.2 High Precision Cleaning

To avoid crosstalk between devices, it is advised to remove the semiconductor between devices. This can be achieved by careful use of the pointed (high precision) cleanroom swabs. **Figure 4.2** shows what the completed test chip should look like after wiping.

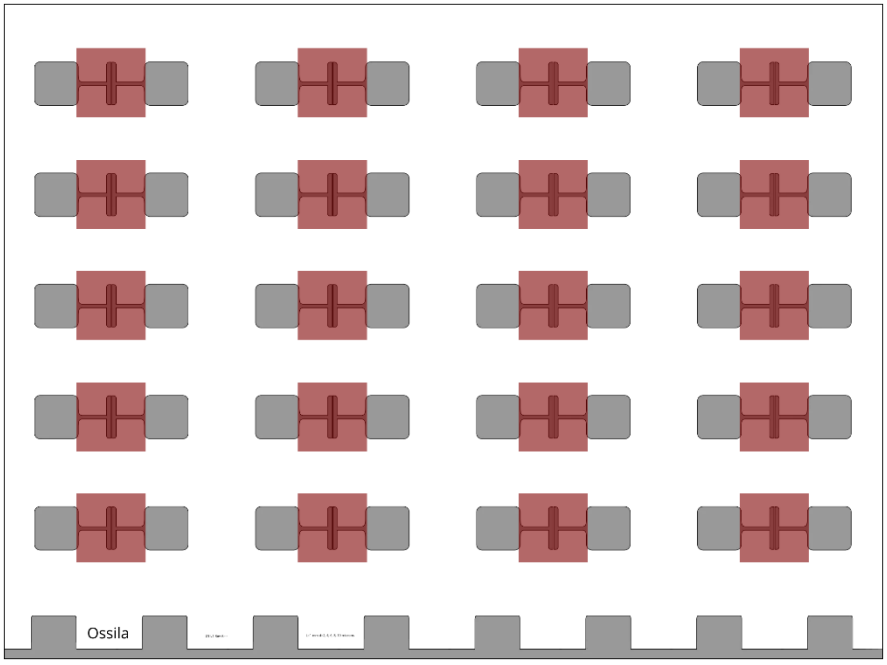

Figure 4.2. Visualisation of OFET test chip after high precision cleaning.

5. Related Products

ITO Coated Substrates

Measure 20 OFETs on a single substrate to help achieve more reliable, statistical results faster.

Product codes: P2014A1

Flat Tip Tweezers

Provides a good substrate grip without scratching.

Product code: C121

Annealing and Cleaning Beaker

Polypropylene beakers with glass lids designed to fit our substrate racks and reduce solvent use.

Product codes: C191

Substrate Cleaning Rack

Holds 20 substrates for a variety of processing techniques.

Product code: E101

UV Ozone Cleaner

For removing contamination on the surface of samples, providing you with ultraclean surfaces within minutes.

Product code: L2002A2

Source Measure Unit

Source voltage, measure current, get data. Simplify and accelerate your data collection!

Product code: P2005A2